

TVL SC70 04 AC0 Engineering Specification

1. Scope

TVL SC70 04 AC0's are TVS arrays designed to protect high-speed signal lines from overvoltage hazard of Electrostatic Discharge (**ESD**), Electrical Fast Transients (**EFT**) and **Lightning**. These interfaces can be used for USB2.0 power and data lines protection, notebook and personal computers, monitors and flat panel displays, IEEE 1394 Firewire Ports, etc.

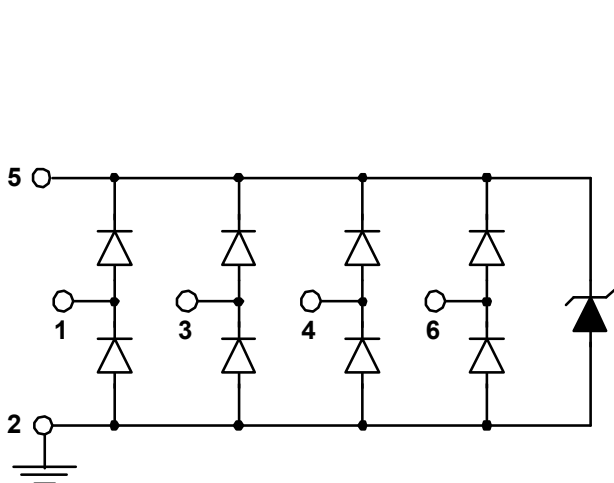
TVL SC70 04 AC0 incorporates a pair of rail-to-rail diodes with low capacitance for each of four I/O channels. Additional Zener diode is employed to minimize the influence of supply voltage. The ESD protection of TVS arrays meets the immunity standard of IEC 61000-4-2, level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

2. Explanation of Part Number

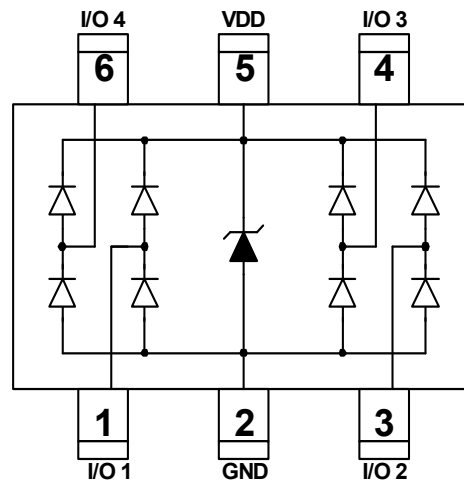
<u>TV</u>	<u>L</u>	<u>SC70</u>	<u>04</u>	<u>AC0</u>
(1)	(2)	(3)	(4)	(5)

- (1) Product Type : TV=TVS Diode
- (2) Capacitance Code : L=Low Capacitance
- (3) Package Size Code
- (4) Channel Code : 04=4 Channels
- (5) Specialized Specification Code

3. Circuit Diagram /Pin Configuration



Circuit Diagram



Pin Configuration
SC70-6L (Top View)

4. Specifications

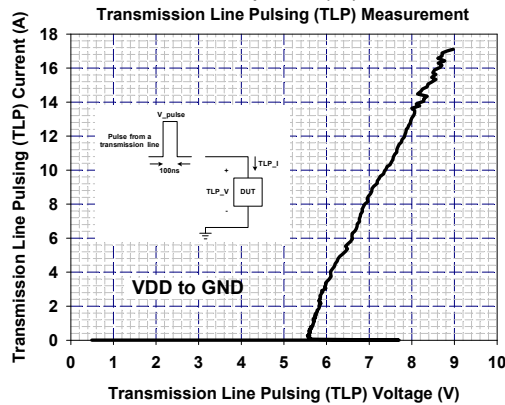
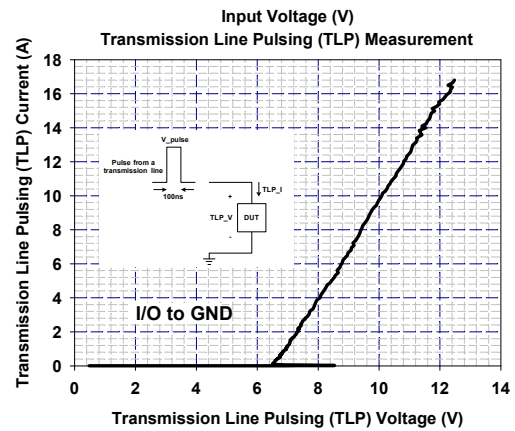
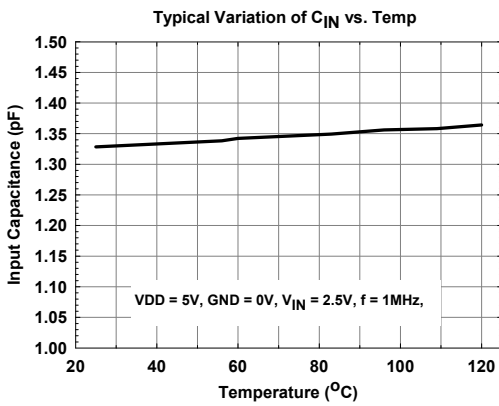
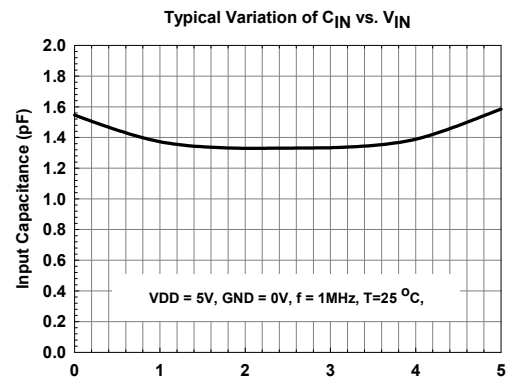
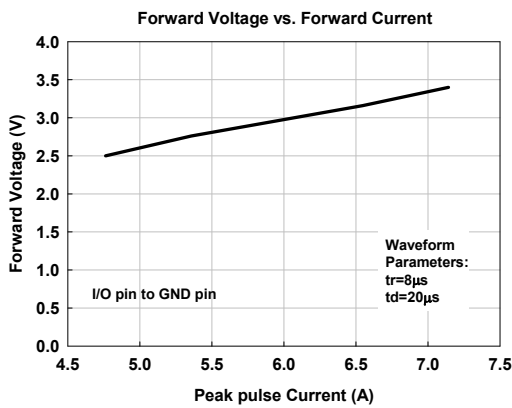
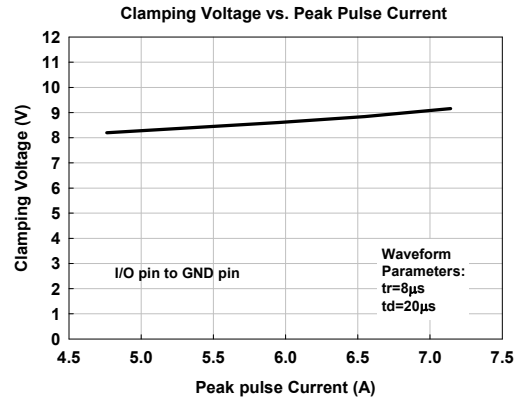
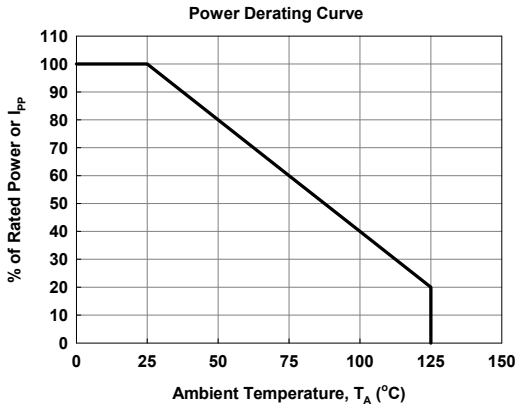
4.1. ABSOLUTE MAXIMUM RATINGS

PARAMETER	PARAMETER	RATING	UNITS
Rated Power	P	150	W
Peak Pulse Current (tp =8/20μs)	I _{PP}	6.5	A
Operating Supply Voltage (VDD-GND)	V _{DC}	6	V
ESD per IEC 61000-4-2 (Air)	V _{ESD}	17	kV
ESD per IEC 61000-4-2 (Contact)		12	
ESD per IEC 61000-4-2(Air)(VDD-GND)	V _{ESD_VDD}	30	kV
ESD per IEC 61000-4-2(Contact) (VDD-GND)		30	
Lead Soldering Temperature	T _{SOL}	260 (10 sec.)	°C
Operating Temperature	T _{OP}	-55 to +85	°C
Storage Temperature	T _{STO}	-55 to +150	°C
DC Voltage at any I/O pin	V _{IO}	(GND – 0.5) to (VDD + 0.5)	V

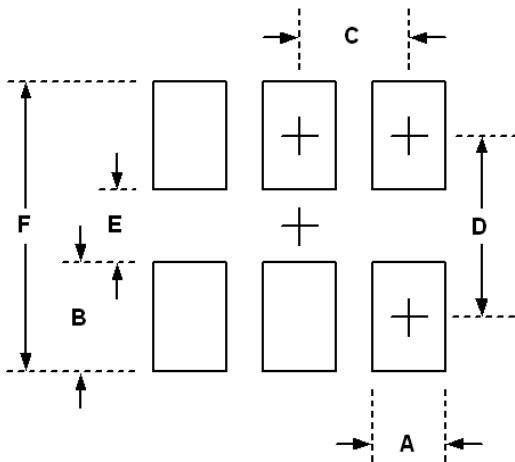
4.2. ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V _{RWM}	Pin 5 to pin 2, T=25 °C			5	V
Reverse Leakage Current	I _{Leak}	V _{RWM} = 5V, T=25 °C, Pin 5 to pin 2			5	μA
Channel Leakage Current	I _{CH_Leak}	V _{Pin 5} = 5V, V _{Pin 2} = 0V, T=25 °C, V _{CH} = 0 ~ 5V			1	μA
Reverse Breakdown Voltage	V _{BV}	I _{BV} = 1mA, T=25 °C Pin 5 to Pin 2	6		9	V
Forward Voltage	V _F	I _F = 15mA, T=25 °C Pin 2 to Pin 5		0.8	1	V
Clamping Voltage	V _{CL}	I _{PP} =5A, tp=8/20μs, T=25 °C Any Channel pin to Ground		8.1	9	V
ESD Clamping Voltage –I/O	V _{clamp_io}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, Any Channel pin to Ground		12.5		V
ESD Clamping Voltage –VDD	V _{clamp_VDD}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, VDD pin to Ground		9		V
ESD Dynamic Turn-on Resistance –I/O	R _{dynamic_io}	IEC 61000-4-2 0~+6kV, T=25 °C, Contact mode, Any Channel pin to Ground		0.35		Ω
ESD Dynamic Turn-on Resistance –VDD	R _{dynamic_VDD}	IEC 61000-4-2 0~+6kV, T=25 °C, Contact mode, VDD pin to Ground		0.2		Ω
Channel Input Capacitance	C _{IN}	V _{pin5} = 5V, V _{pin2} = 0V, V _{IN} = 2.5V, f = 1MHz, T=25 °C, Any Channel pin to Ground		1.3	1.6	pF
Channel to Channel Input Capacitance	C _{CROSS}	V _{pin5} = 5V, V _{pin2} = 0V, V _{IN} = 2.5V, f = 1MHz, T=25 °C, Between Channel pins		0.12	0.14	pF
Variation of Channel Input Capacitance	ΔC _{IN}	V _{pin5} = 5V, V _{pin2} = 0V, V _{IN} = 2.5V, f = 1MHz, T=25 °C, Channel_x pin to Ground - Channel_y pin to Ground		0.05	0.07	pF

4.3. TYPICAL CHARACTERISTICS



5. LAND LAYOUT



Dimensions		
Index	Millimeter	Inches
A	0.35	0.014
B	0.9	0.035
C	0.65	0.025
D	1.6	0.063
E	0.7	0.028
F	2.50	0.098

Notes: This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

6. Application information

A. Design Considerations

The ESD protection scheme for system I/O connector is shown in the Fig. 1. In Fig. 1, the diodes D1 and D2 are general used to protect data line from ESD stress pulse. If the power-rail ESD clamping circuit is not placed between VDD and GND rails, the positive pulse ESD current (I_{ESD1}) will pass through the ESD current path1. Thus, the ESD clamping voltage V_{CL} of data line can be described as follow:

$$V_{CL} = \text{Fwd voltage drop of D1} + \text{supply voltage of VDD rail} + L_1 \times d(I_{ESD1})/dt + L_2 \times d(I_{ESD1})/dt$$

Where L_1 is the parasitic inductance of data line, and L_2 is the parasitic inductance of VDD rail.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30A in 1ns. Here $d(I_{ESD1})/dt$ can be approximated by $\Delta I_{ESD1}/\Delta t$, or $30/(1 \times 10^{-9})$. So just 10nH of total parasitic inductance (L_1 and L_2 combined) will lead to over 300V increment in V_{CL} ! Besides, the ESD pulse current which is directed into the VDD rail may potentially damage any components that are attached to that rail. Moreover, it is common for the forward voltage drop of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. Of course, the discrete diode is also possible to be destroyed due to its power dissipation capability is exceeded.

The TVL SC70 04 AC0 has an integrated power-rail ESD clamped circuit between VDD and GND rails. It can successfully overcome previous disadvantages. During an ESD event, the positive ESD pulse current (I_{ESD2}) will be directed through the integrated power-rail ESD clamped circuit to GND rail (ESD current path2). The clamping voltage V_{CL} on the data line is small and protected IC will not be damaged because power-rail ESD clamped circuit offer a low impedance path to discharge ESD pulse current.

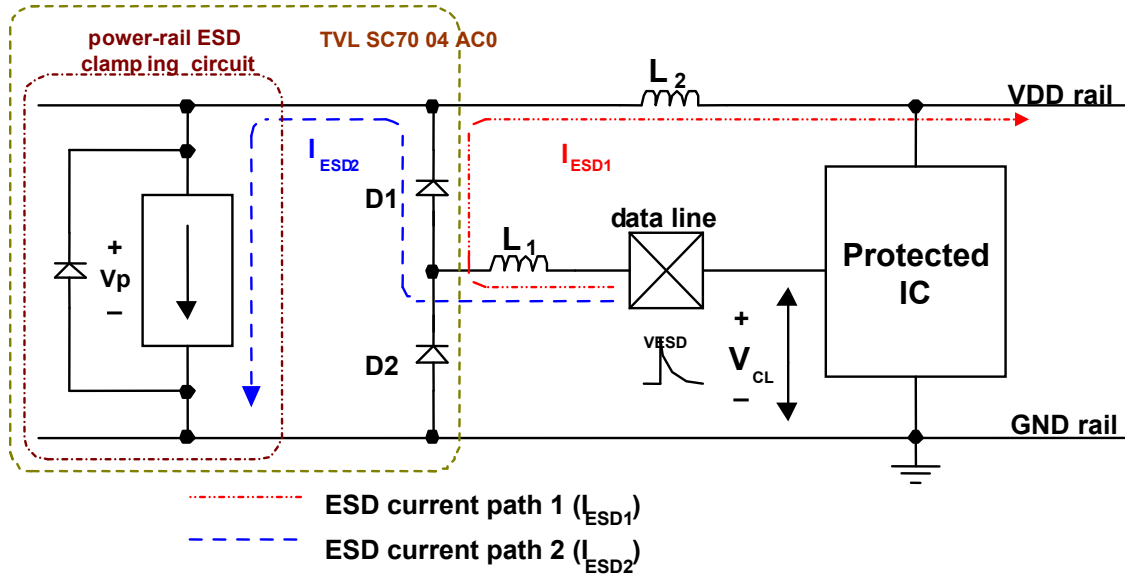
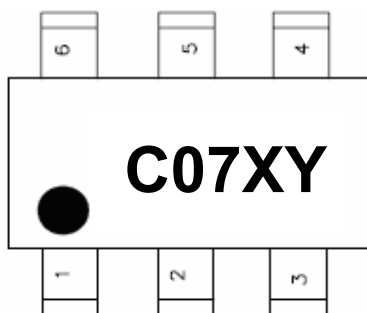


Fig. 1 Application of positive ESD pulse between data line and GND rail.

7. MARKING CODE

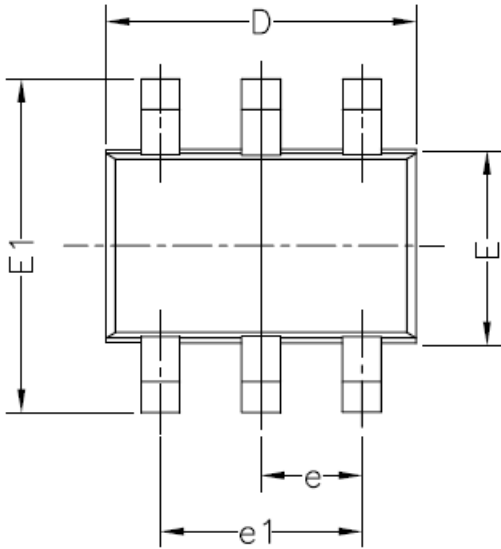
Marking Code: C07XY



C07 = Device Code
 X = Date Code
 Y = Control Code

8. Mechanical Details

SC70-6L PACKAGE DIAGRAMS



PACKAGE DIMENSIONS

Symbol	Milimeters	
	MIN.	MAX.
A	0.90	1.10
A1	0.00	0.10
A2	0.875	1.00
b	0.15	0.40
C	0.08	0.15
D	1.90	2.20
E	1.15	1.35
E1	2.00	2.45
e	0.65 BSC	
e1	1.30 BSC	
L	0.525 REF	
L1	0.26	0.46
L2	0.20 REF	
θ	0°	8°

